WHAT IS CLAIMED IS:

1. A semiconductor device, in which a semiconductor element with an integrated circuit is secured to a board,

wherein the semiconductor element is secured level and specified to operate normally only when the semiconductor element is level.

2. The semiconductor device as defined in claim 1,

wherein the semiconductor element is of a flipped-chip mounting type.

3. The semiconductor device as defined in claim 1,

wherein the semiconductor element receives such stress as a result of processing at least a part of a back thereof that when the semiconductor element is detached from the board, the semiconductor element at least partially deforms due to the stress.

4. The semiconductor device as defined in claim 3,

wherein the semiconductor element has a thickness of 50 μm or less where the semiconductor element is processed.

5. The semiconductor device as defined in claim 3,

wherein the semiconductor element is specified to include a transistor section where transistors are provided at high density, the transistor section at least partially deforming convexly or concavely due to the stress.

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6. The semiconductor device as defined in claim 1,

wherein the semiconductor element includes detector means for detecting an electrical property developing in a level part only when the semiconductor element is level, so as to control operation of the integrated circuit.

7. A method of manufacturing a semiconductor device, comprising, after securing a semiconductor element with an integrated circuit to a board so as to be level, the step of processing at least a part of a back of the semiconductor element to develop such stress that when the semiconductor element is detached from the board, at least a part thereof deforms.

8. The method of manufacturing a semiconductor device as defined in claim 7,

wherein the processing step is specified to be carried out by at least one technique selected from the

group consisting of scraping by means of dicing, sand blast, and sandpaper and treatment by means of laser beam projection.

9. The method of manufacturing a semiconductor device as defined in claim 7,

wherein the processing step is specified to render the semiconductor element have a thickness of 50 μm or less where the semiconductor element is processed.

10. A semiconductor device including a semiconductor element secured to a board, comprising:

a detector section for detecting detachment of the semiconductor element from the board; and

an operation prohibition section for prohibiting operation of the semiconductor element when the detector section has detected the detachment of the semiconductor element from the board.

11. The semiconductor device as defined in claim 10,

wherein:

the semiconductor element is specified to deform when detached from the board; and

the detector section is specified to detect the detachment of the semiconductor element from the board

through detection of the deformation of the semiconductor element.

12. The semiconductor device as defined in claim 11, wherein:

the semiconductor element includes a transistor having an electrical property changing according to the deformation of the semiconductor element; and

the detector section is specified to detect the deformation of the semiconductor element through detection of the change in the electrical property of the transistor.

13. The semiconductor device as defined in claim 12, wherein:

the detector section is specified to output an operation signal to the operation prohibition section when the electrical property of the transistor does not change and to stop the output of the operation signal when the electrical property of the transistor changes; and

the operation prohibition section is specified not to prohibit the operation of the semiconductor element only while receiving the operation signal.

14. The semiconductor device as defined in claim 12, wherein the transistor is of either an NMOS or PMOS type.

15. The semiconductor device as defined in claim 10, wherein the operation prohibition section is specified to prohibit operation of an integrated circuit provided in the semiconductor element.

16. The semiconductor device as defined in claim 10, wherein the detector section and the operation prohibition section are formed on the semiconductor element.

17. The semiconductor device as defined in claim 11, wherein the semiconductor element, when secured to the board, receives such stress that could otherwise deform the semiconductor element.

18. The semiconductor device as defined in claim 17, wherein the semiconductor element is at least partially subjected to rough surface processing when the semiconductor element is secured to the board.

19. The semiconductor device as defined in claim 18,

wherein the semiconductor element has a thickness of 50 μm or less where the semiconductor element is subjected to the rough surface processing.

20. The semiconductor device as defined in claim 18, wherein the semiconductor element has a thickness of 30 μm to 50 μm where the semiconductor element is subjected to the rough surface processing.

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